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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ELLIS, RICHARD L	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,742	WANG ET AL.	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-82* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-82* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20040402*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1 Claims 25-82 are presented for examination.

2 It is noted that applicant's amendment of July 14, 2004 is not properly compliant with 37 CFR 1.121. Applicant filed two preliminary amendments in this application, one filed April 2, 2004, and another filed July 14, 2004. The amendment filed April 2, 2004 canceled original claims 1-24, and submitted new claims 25-39. Subsequently, applicant's amendment of July 14, 2004 resubmitted claims 25-39, and additionally added new claims 40-82. However, in applicant's second amendment (filed July 14, 2004) applicant labeled claims 25-39 with the parenthetical (original) which is improper. A claim may only be labeled (original) when it was first filed with the specification as the last pages thereof. A claim submitted in a preliminary amendment, even if submitted on the same day as the application, is not an originally filed claim, but a newly filed claim. Accordingly, in applicant's amendment of July 14, 2004, claims 25-39 should have been labeled (previously presented) to indicate that they were new in a previous amendment, but were not changed in this amendment. Please see the attached information flyer.

3 The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornam*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground

provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a Terminal Disclaimer. A Terminal Disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4 Claims 1-10 of patent 5,826,055 contain every element of claims 25-32 of the instant application and as such anticipate claims 25-32 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. *In re Longi*, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); *In re Berg*, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus." *Eli Lilly and Company v. Barr Laboratories, Inc.*, United States Court of Appeals for the Federal Circuit, on petition for rehearing en banc (Decided: May 30, 2001).

5,826,055 - Claim 1	***10/816,742 - Claim 25***
1. A superscalar processor that executes a group of instructions out of a program order, the superscalar processor comprising:	25. (Original) A method for retiring instructions in a processor that executes a group of instructions, one or more of the group of instructions executed out of a program order, comprising:
means for assigning tags to instructions;	assigning tags to instructions,
an index-addressable temporary buffer for storing results of executed instructions,	storing results of executed instructions in an index-addressable temporary buffer,
wherein at least part of a tag assigned to an instruction indicates a location in said index-addressable temporary buffer where	wherein at least part of a tag assigned to an instruction indicates a location in said index-addressable temporary buffer where

5,826,055 - Claim 1	*10/816,742 - Claim 25*
an execution result for the instruction is to be stored;	an execution result for the instruction is to be stored;
a register array for storing results of instructions that are retirable;	
means for determining whether an executed instruction is retirable,	determining whether an executed instruction is retirable,
wherein an executed instruction is retirable if there are no unexecuted instructions appearing earlier in program order relative to said executed instruction; and	
means, coupled to said temporary buffer and said register array, for retiring approximately simultaneously a group of retirable instructions by transferring execution results of said group of retirable instructions from said index-addressable temporary buffer to said register array,	and retiring approximately simultaneously a group of retirable instructions, wherein said retiring comprises transferring execution results of said group of retirable instructions from said index-addressable temporary buffer to a register array,
wherein said execution results of said group of retirable instructions are retrieved from said index-addressable temporary buffer based on at least part of each tag assigned to an instruction in said group of retirable instructions.	wherein said execution results of said group of retirable instructions are retrieved from said index-addressable temporary buffer based on at least part of each tag assigned to an instructions in said group of retirable instructions.

5 Claims 11-18 of patent 5,826,055 contain every element of claims 25-32 of the instant application and as such anticipate claims 25-32 of the instant application.

5,826,055 - Claim 11	*10/815,742 - Claim 25*
11. A method for retiring instructions in a processor which executes a group of instructions out of a program order, comprising the steps of:	25. (Original) A method for retiring instructions in a processor that executes a group of instructions, one or more of the group of instructions executed out of a program order, comprising:
(1) assigning tags to instructions;	assigning tags to instructions,
(2) determining whether an executed instruction is retirable,	determining whether an executed instruction is retirable,

5,826,055 - Claim 11	*10/815,742 - Claim 25*
wherein an executed instruction is retirable if there are no unexecuted instructions appearing earlier in program order relative to said executed instruction;	
(3) storing results of executed instructions in an index-addressable temporary buffer addressed by said tags,	storing results of executed instructions in an index-addressable temporary buffer,
wherein at least part of a tag assigned to an instruction indicates a location in said index-addressable temporary buffer where an execution result for the instruction is to be stored; and	wherein at least part of a tag assigned to an instruction indicates a location in said index-addressable temporary buffer where an execution result for the instruction is to be stored; and
(4) retiring approximately simultaneously a group of retirable instructions,	retiring approximately simultaneously a group of retirable instructions,
wherein said step of retiring comprises the step of transferring execution results of said group of retirable instructions from said index-addressable temporary buffer to a register array,	wherein said retiring comprises transferring execution results of said group of retirable instructions from said index-addressable temporary buffer to a register array,
wherein said execution results of said group of retirable instructions are retrieved from said index-addressable temporary buffer based on at least part of each tag assigned to an instruction in said group of retirable instructions.	wherein said execution results of said group of retirable instructions are retrieved from said index-addressable temporary buffer based on at least part of each tag assigned to an instructions in said group of retirable instructions.

6 Claims 11-18 of patent 5,826,055 contain every element of claims 33-39 of the instant application and as such anticipate claims 33-39 of the instant application.

5,826,055 - Claim 11	*10/815,742 - Claim 33*
11. A method for retiring instructions in a processor which executes a group of instructions out of a program order, comprising the steps of:	33. (Original) A method for retiring instructions in a processor that executes a group of instructions, one or more of the group of instructions executed out of a program order, comprising, wherein at least one of said instructions is

5,826,055 - Claim 11	*10/815,742 - Claim 33*
	executed out of a program order;
(1) assigning tags to instructions;	
(2) determining whether an executed instruction is retirable,	determining whether an executed instruction is retirable,
wherein an executed instruction is retirable if there are no unexecuted instructions appearing earlier in program order relative to said executed instruction;	
(3) storing results of executed instructions in an index-addressable temporary buffer addressed by said tags,	storing results of executed instructions in a temporary buffer,
wherein at least part of a tag assigned to an instruction indicates a location in said index-addressable temporary buffer where an execution result for the instruction is to be stored; and	
(4) retiring approximately simultaneously a group of retirable instructions,	
wherein said step of retiring comprises the step of transferring execution results of said group of retirable instructions from said index-addressable temporary buffer to a register array,	transferring execution results of at least one instruction from said temporary buffer to a register array; and
wherein said execution results of said group of retirable instructions are retrieved from said index-addressable temporary buffer based on at least part of each tag assigned to an instruction in said group of retirable instructions.	transferring at least one execution result directly from a functional unit to said register array.

7 Claims 19-27 of patent 5,826,055 contain every element of claims 33-39 of the instant application and as such anticipate claims 33-39 of the instant application.

5,826,055 - Claim 19	*10/815,742 - Claim 33*
19. A superscalar processor that executes a	33. (Original) A method for retiring

5,826,055 - Claim 19	*10/815,742 - Claim 33*
group of instructions out of a program order, the superscalar processor comprising:	instructions in a processor that executes a group of instructions, one or more of the group of instructions executed out of a program order, comprising,
means for determining whether an executed instruction is retirable,	determining whether an executed instruction is retirable,
wherein an executed instruction is considered retirable if there are no unexecuted instructions appearing earlier in a program order;	
a temporary buffer for storing results of instructions that are executed,	storing results of executed instructions in a temporary buffer,
at least one of said instructions being executed out of a program order;	wherein at least one of said instructions is executed out of a program order;
a register array that stores execution results of retirable instructions,	
said register array receiving execution results that are transferred from said temporary buffer,	transferring execution results of at least one instruction from said temporary buffer to a register array;
said register array further receiving execution results that are transferred directly from a functional unit.	and transferring at least one execution result directly from a functional unit to said register array.

8 Claims 28-34 of patent 5,826,055 contain every element of claims 33-39 of the instant application and as such anticipate claims 33-39 of the instant application.

5,826,055 - Claim 28	*10/815,742 - Claim 33*
28. A method for retiring instructions in a processor which executes a group of instructions out of a program order, comprising the steps of:	33. (Original) A method for retiring instructions in a processor that executes a group of instructions, one or more of the group of instructions executed out of a program order, comprising,
(1) determining whether an executed instruction is retirable,	determining whether an executed instruction is retirable,
wherein an executed instruction is retirable	

5,826,055 - Claim 28	*10/815,742 - Claim 33*
if there are no unexecuted instructions appearing earlier in a program order;	
(2) storing results of executed instructions in a temporary buffer,	storing results of executed instructions in a temporary buffer,
wherein at least one of said instructions is executed out of a program order;	wherein at least one of said instructions is executed out of a program order;
(3) transferring execution results of at least one instruction from said temporary buffer to a register array; and	transferring execution results of at least one instruction from said temporary buffer to a register array; and
(4) transferring at least one execution result directly from a functional unit to said register array.	transferring at least one execution result directly from a functional unit to said register array.

9 Claims 1-10 of patent 6,131,157 contain every element of claims 25-32 of the instant application and as such anticipate claims 25-32 of the instant application.

6,131,157 - Claim 1	*10/815,742 - Claim 25*
1. A superscalar processor that executes a group of instructions out of a program order, the superscalar processor comprising:	25. (Original) A method for retiring instructions in a processor that executes a group of instructions, one or more of the group of instructions executed out of a program order, comprising:
a register renaming circuit that assigns tags to instructions;	Assigning tags to instructions,
an index-addressable temporary buffer that stores results of executed instructions,	storing results of executed instructions in an index-addressable temporary buffer,
wherein at least part of a tag assigned to an instruction indicates a location in said index-addressable temporary buffer where an execution result for the instruction is to be stored;	wherein at least part of a tag assigned to an instruction indicates a location in said index-addressable temporary buffer where an execution result for the instruction is to be stored; and
a register array that stores results of instructions that are retirable;	
data dependency checking logic that determines whether an executed instruction is retirable,	determining whether an executed instruction is retirable,
wherein an executed instruction is retirable if there are no unexecuted instructions	

6,131,157 - Claim 1	*10/815,742 - Claim 25*
appearing earlier in program order relative to said executed instruction; and	
an instruction retirement unit that retires approximately simultaneously a group of retirable instructions	retiring approximately simultaneously a group of retirable instructions,
by transferring execution results of said group of retirable instructions from said index-addressable temporary buffer to said register array,	wherein said retiring comprises transferring execution results of said group of retirable instructions from said index-addressable temporary buffer to a register array,
wherein said execution results of said group of retirable instructions are retrieved from said index-addressable temporary buffer based on at least part of each tag assigned to an instruction in said group of retirable instructions.	wherein said execution results of said group of retirable instructions are retrieved from said index-addressable temporary buffer based on at least part of each tag assigned to an instructions in said group of retirable instructions.

10 Claims 11-19 of patent 6,131,157 contain every element of claims 33-39 of the instant application and as such anticipate claims 33-39 of the instant application.

6,131,157 - Claim 11	*10/815,742 - Claim 33*
11. A superscalar processor that executes a group of instructions out of a program order, the superscalar processor comprising:	33. (Original) A method for retiring instructions in a processor that executes a group of instructions, one or more of the group of instructions executed out of a program order, comprising,
data dependency checking logic that determines whether an executed instruction is retirable,	determining whether an executed instruction is retirable,
wherein an executed instruction is considered retirable if there are no unexecuted instructions appearing earlier in a program order;	
a temporary buffer that stores results of instructions that are executed,	storing results of executed instructions in a temporary buffer,
at least one of said instructions being executed out of a program order; and	wherein at least one of said instructions is executed out of a program order;

6,131,157 - Claim 11	*10/815,742 - Claim 33*
a register array that stores execution results of retirable instructions,	
said register array receiving execution results that are transferred from said temporary buffer,	transferring execution results of at least one instruction from said temporary buffer to a register array; and
said register array further receiving execution results that are transferred directly from a functional unit.	transferring at least one execution result directly from a functional unit to said register array.

11 Claims 20-28 of patent 6,131,157 contain every element of claims 33-39 of the instant application and as such anticipate claims 33-39 of the instant application.

6,131,157 - Claim 20	*10/815,742 - Claim 33*
20. A computer system, comprising: a memory unit having stored therein program instructions; and a processor that receives said program instructions via a bus, wherein said processor comprises an instruction retirement system, including	33. (Original) A method for retiring instructions in a processor that executes a group of instructions, one or more of the group of instructions executed out of a program order, comprising,
data dependency checking logic that determines whether an executed instruction is retirable,	determining whether an executed instruction is retirable,
wherein an executed instruction is retirable if there are no unexecuted instructions appearing earlier in a program order;	
a temporary buffer that stores results of executed instructions,	storing results of executed instructions in a temporary buffer,
wherein at least one of said instructions is being executed out of a program order; and	wherein at least one of said instructions is executed out of a program order;
a register array that stores execution results of retirable instructions, from said temporary buffer,	transferring execution results of at least one instruction from said temporary buffer to a register array;
wherein said register array further receives execution results directly from a functional unit.	and transferring at least one execution result directly from a functional unit to said register array.

12 Claims 1-11 of patent 6,412,064 contain every element of claims 25-32 of the instant application and as such anticipate claims 25-32 of the instant application.

6,412,064 - Claim 1	*10/815,742 - Claim 25*
1. A superscalar processor that executes a group of instructions, one of more of the group of instructions executed out of a program order, the superscalar processor comprising:	25. (Original) A method for retiring instructions in a processor that executes a group of instructions, one or more of the group of instructions executed out of a program order, comprising:
a register renaming circuit that assigns tags to instructions;	assigning tags to instructions,
an index-addressable temporary buffer that stores results of executed instructions,	storing results of executed instructions in an index-addressable temporary buffer,
wherein at least part of a tag assigned to an instruction indicates a location in said index-addressable temporary buffer where an execution result for the instruction is to be stored;	wherein at least part of a tag assigned to an instruction indicates a location in said index-addressable temporary buffer where an execution result for the instruction is to be stored; and
a register array that stores results of instructions that are retirable;	
data dependency checking logic that determines whether an executed instruction is retirable; and	determining whether an executed instruction is retirable,
an instruction retirement unit that retires approximately simultaneously a group of retirable instructions	retiring approximately simultaneously a group of retirable instructions,
by transferring execution results of said group of retirable instructions from said index-addressable temporary buffer to said register array,	wherein said retiring comprises transferring execution results of said group of retirable instructions from said index-addressable temporary buffer to a register array,
wherein said execution results of said group of retirable instructions are retrieved from said index-addressable temporary buffer based on at least part of each tag assigned to an instruction in said group of	wherein said execution results of said group of retirable instructions are retrieved from said index-addressable temporary buffer based on at least part of each tag assigned to an instructions in said group of

6,412,064 - Claim 1	*10/815,742 - Claim 25*
retirable instructions.	retirable instructions.

13 Claims 12-21 of patent 6,412,064 contain every element of claims 33-39 of the instant application and as such anticipate claims 33-39 of the instant application.

6,412,064 - Claim 12	*10/815,742 - Claim 33*
12. A superscalar processor that executes a group of instructions, one of more of the group of instructions executed out of a program order, the superscalar processor comprising:	33. (Original) A method for retiring instructions in a processor that executes a group of instructions, one or more of the group of instructions executed out of a program order, comprising,
data dependency checking logic that determines whether an executed instruction is retirable;	determining whether an executed instruction is retirable,
a temporary buffer that stores results of instructions that are executed,	storing results of executed instructions in a temporary buffer,
at least one of said instructions being executed out of a program order; and	wherein at least one of said instructions is executed out of a program order;
a register array that stores execution results of retirable instructions,	
said register array receiving execution results that are transferred from said temporary buffer,	transferring execution results of at least one instruction from said temporary buffer to a register array; and
said register array further receiving execution results that are transferred directly from a functional unit.	transferring at least one execution result directly from a functional unit to said register array.

14 Claims 22-31 of patent 6,412,064 contain every element of claims 33-39 of the instant application and as such anticipate claims 33-39 of the instant application.

6,412,064 - Claim 22	*10/815,742 - claim 33*
22. A computer system, comprising: a	33. (Original) A method for retiring

6,412,064 - Claim 22	*10/815,742 - claim 33*
memory unit having stored therein program instructions; and a processor that receives said program instructions via a bus, wherein said processor comprises an instruction retirement system, including	instructions in a processor that executes a group of instructions, one or more of the group of instructions executed out of a program order, comprising,
data dependency checking logic that determines whether an executed instruction is retirable;	determining whether an executed instruction is retirable,
a temporary buffer that stores results of executed instructions,	storing results of executed instructions in a temporary buffer,
wherein at least one of said instructions is being executed out of a program order;	wherein at least one of said instructions is executed out of a program order;
and a register array that stores execution results of retirable instructions from said temporary buffer,	transferring execution results of at least one instruction from said temporary buffer to a register array;
wherein said register array further receives execution results directly from a functional unit.	and transferring at least one execution result directly from a functional unit to said register array.

15 Claims 32-41 of patent 6,412,064 contain every element of claims 25-32 of the instant application and as such anticipate claims 25-32 of the instant application.

6,412,064 - Claim 32	*10/815,742 - Claim 25*
32. A computer system, comprising: a memory unit having stored therein program instructions; a bus that transfers said program instructions; and a processor that receives said program instructions from said bus, wherein said processor comprises an instruction retirement system, including	25. (Original) A method for retiring instructions in a processor that executes a group of instructions, one or more of the group of instructions executed out of a program order, comprising:
a register renaming circuit that assigns tags to instructions;	assigning tags to instructions,
an index-addressable temporary buffer that stores results of executed instructions,	storing results of executed instructions in an index-addressable temporary buffer,
wherein at least part of a tag assigned to an	wherein at least part of a tag assigned to an

6,412,064 - Claim 32	*10/815,742 - Claim 25*
instruction indicates a location in said index-addressable temporary buffer where an execution result for the instruction is to be stored;	instruction indicates a location in said index-addressable temporary buffer where an execution result for the instruction is to be stored;
a register array that stores execution results of instructions that are retirable;	
data dependency checking logic that determines whether an executed instruction is retirable; and	determining whether an executed instruction is retirable,
an instruction retirement unit that retires approximately simultaneously a group of retirable instructions	and retiring approximately simultaneously a group of retirable instructions,
by transferring execution results of said group of retirable instructions from said index-addressable temporary buffer to said register array,	wherein said retiring comprises transferring execution results of said group of retirable instructions from said index-addressable temporary buffer to a register array,
wherein said execution results of said group of retirable instructions are retrieved from said index addressable temporary buffer based on at least part of each tag assigned to an instruction in said group of retirable instructions.	wherein said execution results of said group of retirable instructions are retrieved from said index-addressable temporary buffer based on at least part of each tag assigned to an instructions in said group of retirable instructions.

16 Claims 1-11 of patent 6,775,761 contain every element of claims 40-53 of the instant application and as such anticipate claims 40-53 of the instant application.

6,775,761 - Claim 1	*10/815,742 - Claim 40*
1. A superscalar processor configured to execute, out of a program order, one or more instructions from a group of instructions comprising:	40. (New) A superscalar processor configured to execute, out of a program order, a plurality of instructions from a group of instructions, the processor comprising:
a superscalar register renaming circuit configured to associate unique addresses with each instruction from the group of instructions,	a superscalar register renaming circuit configured to associate, unique addresses with each instruction from the group of instructions;

6,775,761 - Claim 1	*10/815,742 - Claim 40*
wherein the superscalar register renaming circuit is also configured to associate respective unique addresses with more than one instruction from the group of instructions approximately simultaneously;	in a superscalar manner,
a plurality of functional units configured to execute instructions from the group of instructions out of the program order;	a plurality of functional units configured to execute instructions from the group of instructions out of the program order,
a buffer configured to store execution results of instructions from the group of instructions,	a buffer configured to store execution results of instructions from the group of instructions,
wherein the unique address associated with each instruction indicates a static location in the buffer where an execution result for each instruction is to be stored;	wherein the unique address associated with each instruction indicates a static location in the buffer where an execution result for each instruction is to be stored,
an array including a plurality of array locations referenced to provide execution results of instructions that have been retired;	an array including a plurality of array locations referenced to provide execution results of instructions that have been retired;
a retirement control block configured to determine whether instructions from the group of instructions that are executed can be retired; and	a retirement control block configured to determine whether instructions from the group of instructions that are executed can be retired;
an instruction retirement unit configured to retire approximately simultaneously a group of instructions that can be retired by approximately simultaneously associating an execution result of each instruction in the group of instructions that can be retired to array locations in the register array,	and a superscalar instruction retirement unit configured to retire, in a superscalar manner, a group of instructions that can be retired by associating a respective array location in the array to an execution result of each instruction in the group of instructions that can be retired,
wherein the execution result of each instruction in the group of instructions that can be retired are respectively stored in static locations in the buffer.	wherein the execution result of each instruction in the group of instructions that can be retired is stored in a respective static location in the buffer.

17 Claims 1-11 of patent 6,775,761 contain every element of claims 68-82 of the instant application and as such anticipate claim68-82 of the instant application.

6,775,761 - Claim 1	*10/815,742 - Claim 68*
1. A superscalar processor configured to execute, out of a program order, one or more instructions from a group of instructions comprising:	68. (New) A computer system including a memory configured to store instructions, the instructions having a program order, the system comprising: a processor coupled to the memory, [a processor is inherently attached to memory in order for it to operate]
a superscalar register renaming circuit configured to associate unique addresses with each instruction from the group of instructions,	the processor comprising a superscalar register renaming portion configured to determine, an address associated with each instruction from a group of instructions;
wherein the superscalar register renaming circuit is also configured to associate respective unique addresses with more than one instruction from the group of instructions approximately simultaneously;	in a superscalar manner,
a plurality of functional units configured to execute instructions from the group of instructions out of the program order;	a plurality of functional units coupled to the buffer and configured to execute instructions from the group of instructions out of the program order;
a buffer configured to store execution results of instructions from the group of instructions,	a buffer coupled to the superscalar register renaming portion and configured to store execution results of instructions from the group of instructions
wherein the unique address associated with each instruction indicates a static location in the buffer where an execution result for each instruction is to be stored;	at locations specified by the address associated with each instruction;
an array including a plurality of array locations referenced to provide execution results of instructions that have been retired;	an array including a plurality of locations configured to identify execution results of instructions that are retired;
a retirement control block configured to determine whether instructions from the group of instructions that are executed can be retired;	a control block portion configured to determine whether instructions that are executed can be retired;
and an instruction retirement unit configured to retire approximately simultaneously a group of instructions that can be retired by approximately	and a superscalar instruction retirement portion coupled to the control block portion and coupled to the array, the superscalar instruction retirement portion configured to

6,775,761 - Claim 1	*10/815,742 - Claim 68*
simultaneously associating an execution result of each instruction in the group of instructions that can be retired to array locations in the register array,	retire, in a superscalar manner, a group of instructions that can be retired by associating a respective array location in the array to an execution result of each instruction in the group of instructions that can be retired,
wherein the execution result of each instruction in the group of instructions that can be retired are respectively stored in static locations in the buffer.	wherein the execution result of each instructions in the group of instructions that can be retired is stored at a respective specified location in the buffer.

18. Claims 12-22 of patent 6,775,761 contain every element of claims 54-67 of the instant application and as such anticipate claims 54-67 of the instant application.

6,775,761 - Claim 12	*10/815,742 - Claim 54*
12. A method for retiring instructions in a superscalar processor configured to execute a group of instructions out of a program order, comprising:	54. (New) A method for retiring instructions in a superscalar processor configured to execute a group of instructions out of a program order, the method comprising:
receiving approximately simultaneously a first instruction and a second instruction,	
wherein the first instruction appears earlier in the program order than the second instruction;	wherein the first instruction appears earlier in the program order than the second instruction;
determining approximately simultaneously a first static location in a buffer where an execution result of the first instruction, when executed, is to be stored and a second static location in the buffer where an execution result of the second instruction, when executed, is to be stored;	determining, in a superscalar manner, a first static location in a buffer where an execution result of a first instruction is to be stored and a second static location in the buffer where an execution result of a second instruction is to be stored,
storing the execution result of the second instruction in the buffer at the second static location;	storing the execution result of the second instruction in the buffer at the second static location;
storing the execution result of the first	storing the execution result of the first

6,775,761 - Claim 12	*10/815,742 - Claim 54*
instruction in the buffer at the first static location wherein the second instruction is executed out of the program order with respect to the first instruction;	instruction in the buffer at the first static location wherein the second instruction is executed out of the program order with respect to the first instruction;
determining whether the first instruction can be retired;	determining whether the first instruction can be retired,
determining whether the second instruction can be retired;	determining whether the second instruction can be retired;
retiring approximately simultaneously the first instruction and the second instruction by approximately simultaneously associating the execution result of the first instruction and the execution result of the second instruction stored in the buffer to locations in an array,	retiring, in a superscalar manner, the first instruction and the second instruction by associating locations in an array to the execution results of the first instruction stored in the buffer and the execution result of the second instruction stored in the buffer,
wherein the execution result of the first instruction and the execution result of the second instruction are respectively identified from the buffer at the first static location and the second static location.	wherein the execution result of the first instruction and the execution result of the second instruction are respectively identified within the buffer at the first static location and the second static location.

19 Claims 23-34 of patent 6,775,761 contain every element of claims 40-53 of the instant application and as such anticipate claims 40-53 of the instant application.

6,775,761 - Claim 23	*10/815,742 - Claim 40*
23. A computer system including a memory configured to store instructions, the instructions having a program order, comprising:	40. (New) A superscalar processor configured to execute, out of a program order, a plurality of instructions from a group of instructions, the processor comprising:
a processor coupled to the memory comprising:	
a superscalar register renaming portion configured to determine an address associated with each instruction from a group of instructions	a superscalar register renaming circuit configured to associate unique addresses with each instruction from the group of instructions;

6,775,761 - Claim 23	*10/815,742 - Claim 40*
wherein the superscalar register renaming portion is also configured to associate addresses with more than one instruction from the group of instructions within a clock cycle;	, in a superscalar manner,
a buffer coupled to the register renaming portion configured to store execution results of instructions from the group of instructions at locations specified by the address associated with each instruction;	a buffer configured to store execution results of instructions from the group of instructions, wherein the unique address associated with each instruction indicates a static location in the buffer where an execution result for each instruction is to be stored,
a plurality of functional units coupled to the buffer and configured to execute instructions from the group of instructions out of the program order;	a plurality of functional units configured to execute instructions from the group of instructions out of the program order,
an array including a plurality of locations configured to identify execution results of instructions that are retired;	an array including a plurality of array locations referenced to provide execution results of instructions that have been retired;
a control block portion configured to determine whether instructions that are executed can be retired;	a retirement control block configured to determine whether instructions from the group of instructions that are executed can be retired;
and an instruction retirement portion coupled to the control block portion and coupled to the array, the instruction retirement portion configured to retire approximately simultaneously a group of instructions that can be retired by approximately simultaneously associating execution results of the group of instructions that can be retired to locations in the array,	and a superscalar instruction retirement unit configured to retire, in a superscalar manner, a group of instructions that can be retired by associating a respective array location in the array to an execution result of each instruction in the group of instructions that can be retired,
wherein the execution results of the group of instructions that can be retired are respectively stored at specified locations in the buffer.	wherein the execution result of each instruction in the group of instructions that can be retired is stored in a respective static location in the buffer.

20 Claims 23-34 of patent 6,775,761 contain every element of claims 68-82 of the instant application and as such anticipate claim 68-82 of the instant application.

6,775,761 - Claim 23	*10/815,742 - Claim 68*
23. A computer system including a memory configured to store instructions, the instructions having a program order, comprising:	68. (New) A computer system including a memory configured to store instructions, the instructions having a program order, the system comprising:
a processor coupled to the memory comprising:	a processor coupled to the memory, the processor comprising
a superscalar register renaming portion configured to determine an address associated with each instruction from a group of instructions wherein the superscalar register renaming portion is also configured to associate addresses with more than one instruction from the group of instructions within a clock cycle;	a superscalar register renaming portion configured to determine, in a superscalar manner, an address associated with each instruction from a group of instructions;
a buffer coupled to the register renaming portion configured to store execution results of instructions from the group of instructions at locations specified by the address associated with each instruction;	a buffer coupled to the superscalar register renaming portion and configured to store execution results of instructions from the group of instructions at locations specified by the address associated with each instruction;
a plurality of functional units coupled to the buffer and configured to execute instructions from the group of instructions out of the program order;	a plurality of functional units coupled to the buffer and configured to execute instructions from the group of instructions out of the program order;
an array including a plurality of locations configured to identify execution results of instructions that are retired;	an array including a plurality of locations configured to identify execution results of instructions that are retired;
a control block portion configured to determine whether instructions that are executed can be retired; and	a control block portion configured to determine whether instructions that are executed can be retired;
an instruction retirement portion coupled to the control block portion and coupled to the array,	and a superscalar instruction retirement portion coupled to the control block portion and coupled to the array,
the instruction retirement portion	the superscalar instruction retirement

6,775,761 - Claim 23	*10/815,742 - Claim 68*
configured to retire approximately simultaneously a group of instructions that can be retired	portion configured to retire, in a superscalar manner, a group of instructions that can be retired
by approximately simultaneously associating execution results of the group of instructions that can be retired to locations in the array,	by associating a respective array location in the array to an execution result of each instruction in the group of instructions that can be retired,
wherein the execution results of the group of instructions that can be retired are respectively stored at specified locations in the buffer.	wherein the execution result of each instructions in the group of instructions that can be retired is stored at a respective specified location in the buffer.

21 Claims 34-40 of patent 6,775,761 contain every element of claims 54-67 of the instant application and as such anticipate claims 54-67 of the instant application.

6,775,761 - Claim 34	*10/815,742 - Claim 54*
34. A method for retiring instructions in a superscalar processor configured to execute a group of instructions out of a program order, comprising:	54. (New) A method for retiring instructions in a superscalar processor configured to execute a group of instructions out of a program order, the method comprising:
concurrently receiving a first instruction and a second instruction,	
wherein the first instruction appears earlier in the program order than the second instruction;	wherein the first instruction appears earlier in the program order than the second instruction;
determining within a clock cycle, a first location in a temporary buffer where an execution result of the first instruction, when executed, is to be stored, and a second location in the temporary buffer where an execution result of the second instruction, when executed, is to be stored;	determining, in a superscalar manner, a first static location in a buffer where an execution result of a first instruction is to be stored and a second static location in the buffer where an execution result of a second instruction is to be stored,
storing the execution result of the second instruction in the temporary buffer at the second location;	storing the execution result of the second instruction in the buffer at the second static location;

6,775,761 - Claim 34	*10/815,742 - Claim 54*
storing the execution result of the first instruction in the temporary buffer at the first location, wherein the second instruction is executed out of the program order with respect to the first instruction;	storing the execution result of the first instruction in the buffer at the first static location wherein the second instruction is executed out of the program order with respect to the first instruction;
determining whether the first instruction can be retired;	determining whether the first instruction can be retired,
determining whether the second instruction can be retired;	determining whether the second instruction can be retired;
retiring approximately simultaneously the first instruction and the second instruction by approximately simultaneously writing the execution result of the first instruction stored at the first location in the temporary buffer in a first location in a register array, and	retiring, in a superscalar manner, the first instruction and the second instruction by associating locations in an array to the execution results of the first instruction stored in the buffer and the execution result of the second instruction stored in the buffer,
writing the execution result of the second instruction stored at the second location in the temporary buffer in a second location in the register array.	wherein the execution result of the first instruction and the execution result of the second instruction are respectively identified within the buffer at the first static location and the second static location.

22 Claims 41-47 of patent 6,775,761 contain every element of claims 40-53 of the instant application and as such anticipate claims 40-53 of the instant application.

6,775,761 - Claim 41	*10/815,742 - Claim 40*
41. A superscalar processor configured to execute, out of a program order, one or more instructions from a group of instructions comprising:	40. (New) A superscalar processor configured to execute, out of a program order, a plurality of instructions from a group of instructions, the processor comprising:
a superscalar register renaming circuit configured to approximately simultaneously associate a first address with a first instruction from the group of instructions and a second address with a second instruction from the group of instructions;	a superscalar register renaming circuit configured to associate, in a superscalar manner, unique addresses with each instruction from the group of instructions;

6,775,761 - Claim 41	*10/815,742 - Claim 40*
a plurality of functional units configured to execute the first instruction and the second instruction from the group of instructions out of the program order;	a plurality of functional units configured to execute instructions from the group of instructions out of the program order,
a temporary buffer configured to store execution results of the first instruction and the second instruction from the group of instructions,	a buffer configured to store execution results of instructions from the group of instructions,
wherein the first address associated with the first instruction indicates a first static location in the temporary buffer where an execution result for the first instruction is to be stored, and wherein the second address associated with the second instruction indicates a second static location in the temporary buffer where an execution result for the second instruction is to be stored;	wherein the unique address associated with each instruction indicates a static location in the buffer where an execution result for each instruction is to be stored,
a register array having a plurality of register array locations configured to store execution results of instructions that have been retired;	an array including a plurality of array locations referenced to provide execution results of instructions that have been retired;
a retirement control block configured to determine whether the first instruction can be retired, and configured to determine whether the second instruction can be retired; and	a retirement control block configured to determine whether instructions from the group of instructions that are executed can be retired;
an instruction retirement unit configured to retire the first instruction and the second instruction by approximately simultaneously storing	and a superscalar instruction retirement unit configured to retire, in a superscalar manner, a group of instructions that can be retired by
the execution result of the first instruction stored in the first static location in the temporary buffer in a first register array location and storing the execution result of the second instruction stored in the second static location in the temporary buffer in a second register array location.	associating a respective array location in the array to an execution result of each instruction in the group of instructions that can be retired, wherein the execution result of each instruction in the group of instructions that can be retired is stored in a respective static location in the buffer.

23 Claims 41-47 of patent 6,775,761 contain every element of claims 54-67 of the instant

application and as such anticipate claims 54-67 of the instant application.

6,775,761 - Claim 41	*10/815,742 - Claim 54*
41. A superscalar processor configured to execute, out of a program order, one or more instructions from a group of instructions comprising:	54. (New) A method for retiring instructions in a superscalar processor configured to execute a group of instructions out of a program order, the method comprising:
a superscalar register renaming circuit configured to approximately simultaneously associate a first address with a first instruction from the group of instructions and a second address with a second instruction from the group of instructions;	determining, in a superscalar manner, a first static location in a buffer where an execution result of a first instruction is to be stored and a second static location in the buffer where an execution result of a second instruction is to be stored,
a plurality of functional units configured to execute the first instruction and the second instruction from the group of instructions out of the program order;	wherein the first instruction appears earlier in the program order than the second instruction; wherein the second instruction is executed out of the program order with respect to the first instruction;
a temporary buffer configured to store execution results of the first instruction and the second instruction from the group of instructions,	
wherein the first address associated with the first instruction indicates a first static location in the temporary buffer where an execution result for the first instruction is to be stored, and	storing the execution result of the first instruction in the buffer at the first static location
wherein the second address associated with the second instruction indicates a second static location in the temporary buffer where an execution result for the second instruction is to be stored;	storing the execution result of the second instruction in the buffer at the second static location;
a register array having a plurality of register array locations configured to store execution results of instructions that have been retired;	
a retirement control block configured to determine whether the first instruction can be retired, and	determining whether the first instruction can be retired,
configured to determine whether the second	determining whether the second instruction

6,775,761 - Claim 41	*10/815,742 - Claim 54*
instruction can be retired; and	can be retired;
an instruction retirement unit configured to retire the first instruction and the second instruction by approximately simultaneously storing the execution result of the first instruction stored in the first static location in the temporary buffer in a first register array location and storing the execution result of the second instruction stored in the second static location in the temporary buffer in a second register array location.	retiring, in a superscalar manner, the first instruction and the second instruction by associating locations in an array to the execution results of the first instruction stored in the buffer and the execution result of the second instruction stored in the buffer, wherein the execution result of the first instruction and the execution result of the second instruction are respectively identified within the buffer at the first static location and the second static location.

24 Claims 25-82 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Nguyen et al., U.S. Patent 5,961,629.

Nguyen et al. discloses every aspect of the invention disclosed in this application, and as such, anticipates the claims of this application.

25 A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

26 Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (571) 272-4165. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (571) 272-4162. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Richard Ellis
October 14, 2004

RICHARD L. ELLIS
PRIMARY EXAMINER

RICHARD L. ELLIS
PRIMARY EXAMINER